

SCAN15MB200

Dual 1.5 Gbps 2:1/1:2 LVDS Mux/Buffer with Pre-Emphasis and IEEE 1149.6

General Description

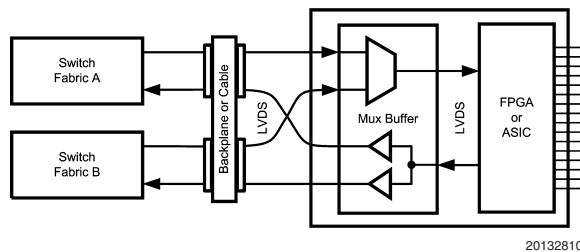
The SCAN15MB200 is a dual-port 2 to 1 multiplexer and 1 to 2 repeater/buffer. High-speed data paths and flow-through pinout minimize internal device jitter and simplify board layout, while pre-emphasis overcomes ISI jitter effects from lossy backplanes and cables. The differential inputs and outputs interface to LVDS or Bus LVDS signals such as those on National's 10-, 16-, and 18-bit Bus LVDS SerDes, or to CML or LVPECL signals.

Integrated IEEE 1149.1 (JTAG) and 1149.6 circuitry supports testability of both single-ended LVTTTL/CMOS and high-speed differential PCB interconnects. The 3.3V supply, CMOS process, and robust I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

Features

- 1.5 Gbps data rate per channel
- Configurable off/on pre-emphasis drives lossy backplanes and cables
- LVDS/BLVDS/CML/LVPECL compatible inputs, LVDS compatible outputs
- Low output skew and jitter
- On-chip 100Ω input and output termination
- IEEE 1149.1 and 1149.6 compliant
- 15 kV ESD protection on LVDS inputs/outputs
- Hot plug Protection
- Single 3.3V supply
- Industrial -40 to +85°C temperature range
- 48-pin LLP Package

Typical Application



Block Diagram

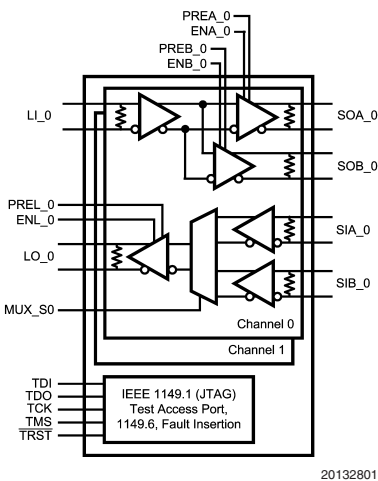


FIGURE 1. SCAN15MB200 Block Diagram

Pin Descriptions			
Pin Name	LLP Pin Number	I/O, Type	Description
SWITCH SIDE DIFFERENTIAL INPUTS			
SIA_0+	30	I, LVDS	Switch A-side Channel 0 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SIA_0-	29		
SIA_1+	19	I, LVDS	Switch A-side Channel 1 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SIA_1-	20		
SIB_0+	28	I, LVDS	Switch B-side Channel 0 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SIB_0-	27		
SIB_1+	21	I, LVDS	Switch B-side Channel 1 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SIB_1-	22		
LINE SIDE DIFFERENTIAL INPUTS			
LI_0+	40	I, LVDS	Line-side Channel 0 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
LI_0-	39		
LI_1+	9	I, LVDS	Line-side Channel 1 inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
LI_1-	10		
SWITCH SIDE DIFFERENTIAL OUTPUTS			
SOA_0+	34	O, LVDS	Switch A-side Channel 0 inverting and non-inverting differential outputs. LVDS compatible (Notes 1, 3).
SOA_0-	33		
SOA_1+	15	O, LVDS	Switch A-side Channel 1 inverting and non-inverting differential outputs. LVDS compatible (Notes 1, 3).
SOA_1-	16		
SOB_0+	32	O, LVDS	Switch B-side Channel 0 inverting and non-inverting differential outputs. LVDS compatible (Notes 1, 3).
SOB_0-	31		
SOB_1+	17	O, LVDS	Switch B-side Channel 1 inverting and non-inverting differential outputs. LVDS compatible (Notes 1, 3).
SOB_1-	18		
LINE SIDE DIFFERENTIAL OUTPUTS			
LO_0+	42	O, LVDS	Line-side Channel 0 inverting and non-inverting differential outputs. LVDS compatible (Notes 1, 3).
LO_0-	41		
LO_1+	7	O, LVDS	Line-side Channel 1 inverting and non-inverting differential outputs. LVDS compatible (Notes 1, 3).
LO_1-	8		
DIGITAL CONTROL INTERFACE			
MUX_S0	38	I, LVTTTL	Mux Select Control Inputs (per channel) to select which Switch-side input, A or B, is passed through to the Line-side.
MUX_S1	11		
PREA_0	26	I, LVTTTL	Output pre-emphasis control for Switch-side outputs. Each output driver on the Switch A-side and B-side has a separate pin to control the pre-emphasis on or off.
PREA_1	23		
PREB_0	25		
PREB_1	24		
PREL_0	44	I, LVTTTL	Output pre-emphasis control for Line-side outputs. Each output driver on the Line A-side and B-side has a separate pin to control the pre-emphasis on or off.
PREL_1	5		
ENA_0	36	I, LVTTTL	Output Enable Control for Switch A-side and B-side outputs. Each output driver on the A-side and B-side has a separate enable pin.
ENA_1	13		
ENB_0	35		
ENB_1	14		
ENL_0	45	I, LVTTTL	Output Enable Control for The Line-side outputs. Each output driver on the Line-side has a separate enable pin.
ENL_1	4		
TDI	2	I, LVTTTL	Test Data Input to support IEEE 1149.1 features
TDO	1	O, LVTTTL	Test Data Output to support IEEE 1149.1 features
TMS	46	I, LVTTTL	Test Mode Select to support IEEE 1149.1 features
TCK	47	I, LVTTTL	Test Clock to support IEEE 1149.1 features
$\overline{\text{TRST}}$	3	I, LVTTTL	Test Reset to support IEEE 1149.1 features
POWER			

Pin Descriptions (Continued)

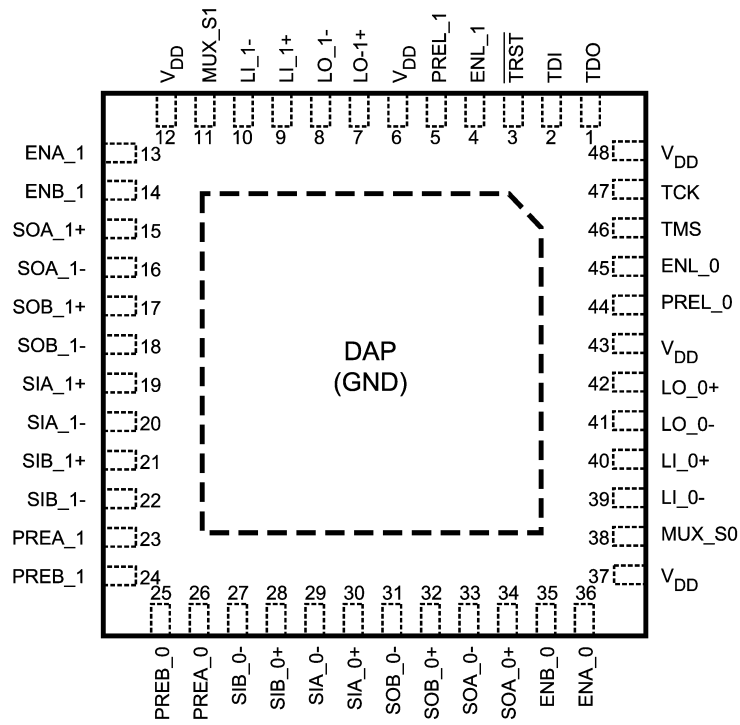
Pin Name	LLP Pin Number	I/O, Type	Description
V _{DD}	6, 12, 37, 43, 48	I, Power	V _{DD} = 3.3V ±0.3V.
GND	(Note 2)	I, Power	Ground reference for LVDS and CMOS circuitry. For the LLP package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the LLP-48 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.

Note 1: For interfacing LVDS outputs to CML or LVPECL compatible inputs, refer to the applications section of this datasheet (planned).

Note 2: Note that the DAP on the backside of the LLP package is the primary GND connection for the device when using the LLP package.

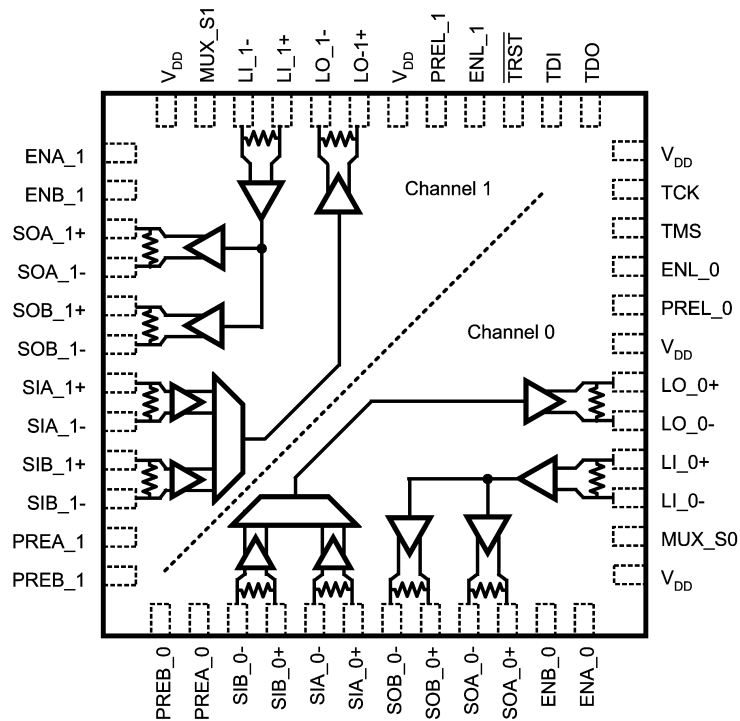
Note 3: The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the SCAN15MB200 device have been optimized for point-to-point backplane and cable applications.

Connection Diagrams



LLP Top View
DAP = GND

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Directional Signal Paths Top View
(Refer to pin names for signal polarity)

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Output Characteristics

The output characteristics of the SCAN15MB200 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

A 100Ω output (source) termination resistor is incorporated in the device to eliminate the need for an external resistor, providing excellent drive characteristics by locating the source termination as close to the output as physically possible.

Pre-Emphasis Controls

The pre-emphasis is used to compensate for long or lossy transmission media. Separate pins are provided for each output to minimize power consumption. Pre-emphasis is programmable to be off or on per the Pre-emphasis Control Table.

PREx_n (Note 4)	Output Pre-emphasis
0	0%
1	100%

Note 4: Applies to PREA_0, PREA_1, PREB_0, PREB_1, PREL_0, PREL_1

Multiplexer Truth Table (Note 5)

Data Inputs		Control Inputs		Output
SIA_0	SIB_0	MUX_S0	ENL_0	LO_0
X	valid	0	1	SIB_0
valid	X	1	1	SIA_0
X	X	X	0 (Note 6)	Z

X = Don't Care

Z = High Impedance (TRI-STATE)

Repeater/Buffer Truth Table (Note 5)

Data Input	Control Inputs		Outputs	
LI_0	ENA_0	ENB_0	SOA_0	SOB_0
X	0	0	Z (Note 6)	Z (Note 6)
valid	0	1	Z	LI_0
valid	1	0	LI_0	Z
valid	1	1	LI_0	LI_0

X = Don't Care

Z = High Impedance (TRI-STATE)

Note 5: Same functionality for channel 1

Note 6: When all enable inputs from both channels are Low, the device enters a powerdown mode. Refer to the applications section titled TRI-STATE and Powerdown modes.

Absolute Maximum Ratings (Note 7)

Supply Voltage (V_{DD})	-0.3V to +4.0V
CMOS Input Voltage	-0.3V to ($V_{DD}+0.3V$)
LVDS Receiver Input Voltage (Note 8)	-0.3V to ($V_{DD}+0.3V$)
LVDS Driver Output Voltage	-0.3V to ($V_{DD}+0.3V$)
LVDS Output Short Circuit Current	+40 mA
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Solder, 4sec)	260°C
Max Pkg Power Capacity @ 25°C	5.2W
Thermal Resistance (θ_{JA})	24°C/W
Package Derating above +25°C	41.7mW/°C
ESD Last Passing Voltage	
HBM, 1.5k Ω , 100pF	8kV
LVDS pins to GND only	15kV

EIAJ, 0 Ω , 200pF

250V

CDM

1000V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Input Voltage (V_I) (Note 8)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
Industrial	-40°C to +85°C

Note 7: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of products outside of recommended operation conditions.

Note 8: V_{ID} max < 2.4V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 9)	Max	Units
LVTTL DC SPECIFICATIONS (MUX_Sn, PREA_n, PREB_n, PREL_n, ENA_n, ENB_n, ENL_n, TDI, TDO, TCK, TMS, TRST)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	-10		+10	μ A
I_{IHR}	High Level Output Current	PREA_n, PREB_n, PREL_n	40		200	μ A
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}, V_{DD} = V_{DDMAX}$	-10		+10	μ A
I_{ILR}	Low Level Input Current	TDI, TMS, TRST	-40		-200	μ A
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		2.0		pF
C_{OUT1}	Output Capacitance	Any Digital Output Pin to V_{SS}		4.0		pF
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA	-1.5	-0.8		V
V_{OH}	High Level Output Voltage (TDO)	$I_{OH} = -12$ mA, $V_{DD} = 3.0$ V	2.4			V
		$I_{OH} = -100$ μ A, $V_{DD} = 3.0$ V	$V_{DD}-0.2$			V
V_{OL}	Low Level Output Voltage (TDO)	$I_{OL} = 12$ mA, $V_{DD} = 3.0$ V			0.5	V
		$I_{OL} = 100$ μ A, $V_{DD} = 3.0$ V			0.2	V
I_{OS}	Output Short Circuit Current	TDO	-15		-125	mA
I_{OZ}	Output TRI-STATE Current	TDO	-10		+10	μ A
LVDS INPUT DC SPECIFICATIONS (SIA \pm , SIB \pm , LI \pm)						
V_{TH}	Differential Input High Threshold (Note 10)	$V_{CM} = 0.8V$ or 1.2V or 3.55V, $V_{DD} = 3.6V$		0	100	mV
V_{TL}	Differential Input Low Threshold (Note 10)	$V_{CM} = 0.8V$ or 1.2V or 3.55V, $V_{DD} = 3.6V$	-100	0		mV
V_{ID}	Differential Input Voltage	$V_{CM} = 0.8V$ to 3.55V, $V_{DD} = 3.6V$	100		2400	mV
V_{CMR}	Common Mode Voltage Range	$V_{ID} = 150$ mV, $V_{DD} = 3.6V$	0.05		3.55	V
C_{IN2}	Input Capacitance	IN+ or IN- to V_{SS}		2.0		pF
I_{IN}	Input Current	$V_{IN} = 3.6V$, $V_{DD} = V_{DDMAX}$ or 0V	-15		+15	μ A
		$V_{IN} = 0V$, $V_{DD} = V_{DDMAX}$ or 0V	-15		+15	μ A

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 9)	Max	Units
LVDS OUTPUT DC SPECIFICATIONS (SOA _{n±} , SOB _{n±} , LO _{n±})						
V _{OD}	Differential Output Voltage, 0% Pre-emphasis (Note 10)	R _L is the internal 100Ω between OUT+ and OUT-	250	360	500	mV
ΔV _{OD}	Change in V _{OD} between Complementary States		-35		35	mV
V _{OS}	Offset Voltage (Note 11)		1.05	1.22	1.475	V
ΔV _{OS}	Change in V _{OS} between Complementary States		-35		35	mV
I _{OS}	Output Short Circuit Current	OUT+ or OUT- Short to GND		-21	-40	mA
C _{OUT2}	Output Capacitance	OUT+ or OUT- to GND when TRI-STATE		4.0		pF
SUPPLY CURRENT (Static)						
I _{CC}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT-.		225	275	mA
I _{CCZ}	Supply Current - Powerdown Mode	ENA ₀ = ENB ₀ = ENL ₀ = ENA ₁ = ENB ₁ = ENL ₁ = L		0.6	4.0	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS						
t _{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V _{OD} . (Note 16)		170	250	ps
t _{HLT}	Differential High to Low Transition Time			170	250	ps
t _{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V _{OD} between input to output.		1.0	2.5	ns
t _{PHLD}	Differential High to Low Propagation Delay			1.0	2.5	ns
t _{SKD1}	Pulse Skew	t _{PLHD} - t _{PHLD} (Note 16)		25	75	ps
t _{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t _{PLHD} or t _{PHLD}) among all output channels. (Note 16)		50	115	ps
t _{JIT}	Jitter (0% Pre-emphasis) (Note 12)	RJ - Alternating 1 and 0 at 750MHz (Note 13)		1.1	1.5	psrms
		DJ - K28.5 Pattern, 1.5 Gbps (Note 14)		20	34	psp-p
		TJ - PRBS 2 ⁷ -1 Pattern, 1.5 Gbps (Note 15)		14	28	psp-p
t _{ON}	LVDS Output Enable Time	Time from ENA _n , ENB _n , or ENL _n to OUT± change from TRI-STATE to active.		0.5	1.5	μs
t _{ON2}	LVDS Output Enable time from powerdown mode	Time from ENA _n , ENB _n , or ENL _n to OUT± change from Powerdown to active		10	20	μs
t _{OFF}	LVDS Output Disable Time	Time from ENA _n , ENB _n , or ENL _n to OUT± change from active to TRI-STATE or powerdown.			12	ns

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 9)	Max	Units
SWITCHING CHARACTERISTICS - SCAN FEATURES						
f_{MAX}	Maximum TCK Clock Frequency	$R_L = 500\Omega,$ $C_L = 35\text{ pF}$	25.0			MHz
t_S	TDI to TCK, H or L		3.0			ns
t_H	TDI to TCK, H or L		0.5			ns
t_S	TMS to TCK, H or L		3.0			ns
t_H	TMS to TCK, H or L		0.5			ns
t_W	TCK Pulse Width, H or L		10.0			ns
t_W	$\overline{\text{TRST}}$ Pulse Width, L		2.5			ns
t_{REC}	Recovery Time, $\overline{\text{TRST}}$ to TCK		2.0			ns

Note 9: Typical parameters are measured at $V_{DD} = 3.3V$, $T_A = 25^\circ\text{C}$. They are for reference purposes, and are not production-tested.

Note 10: Differential output voltage V_{OD} is defined as $\text{ABS}(\text{OUT+} - \text{OUT-})$. Differential input voltage V_{ID} is defined as $\text{ABS}(\text{IN+} - \text{IN-})$.

Note 11: Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

Note 12: Jitter is not production tested, but guaranteed through characterization on a sample basis.

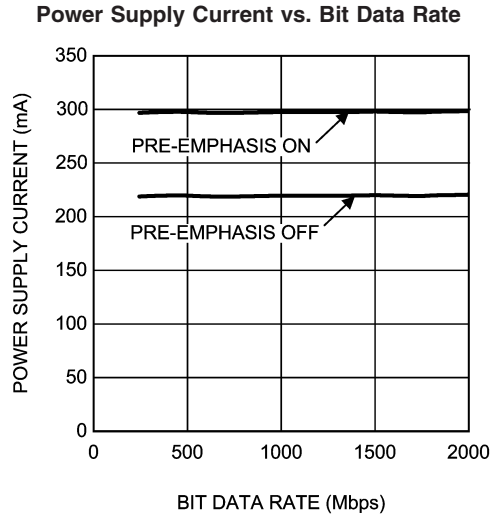
Note 13: Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = $V_{ID} = 500\text{mV}$, 50% duty cycle at 750MHz, $t_r = t_f = 50\text{ps}$ (20% to 80%).

Note 14: Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. Stimulus and fixture jitter has been subtracted. The input voltage = $V_{ID} = 500\text{mV}$, K28.5 pattern at 1.5 Gbps, $t_r = t_f = 50\text{ps}$ (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

Note 15: Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage = $V_{ID} = 500\text{mV}$, 2^{7-1} PRBS pattern at 1.5 Gbps, $t_r = t_f = 50\text{ps}$ (20% to 80%).

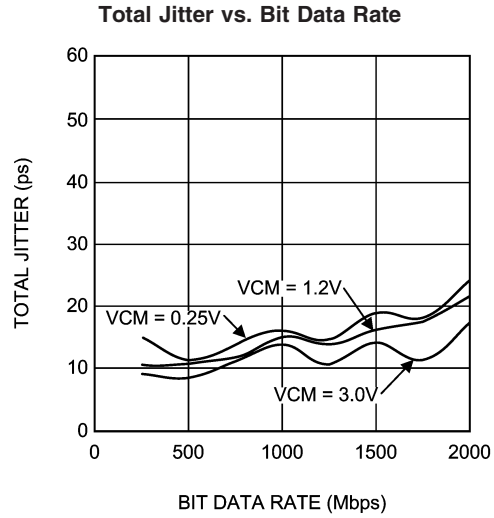
Note 16: Not Production tested. Guaranteed by statistical analysis on a sample basis at the time of characterization.

Typical Performance Characteristics



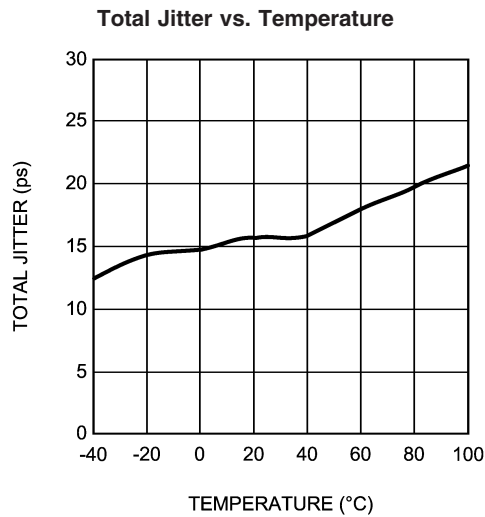
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Dynamic power supply current was measured with all channels active and toggling at the bit data rate. Data pattern has no effect on the power consumption. $V_{DD} = 3.3V$, $T_A = +25^\circ C$, $V_{ID} = 0.5V$, $V_{CM} = 1.2V$



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Total Jitter measured at 0V differential while running a PRBS 2^7-1 pattern with one channel active, all other channels are disabled. $V_{DD} = 3.3V$, $T_A = +25^\circ C$, $V_{ID} = 0.5V$, pre-emphasis off.



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Total Jitter measured at 0V differential while running a PRBS 2^7-1 pattern with one channel active, all other channels are disabled. $V_{DD} = 3.3V$, $V_{ID} = 0.5V$, $V_{CM} = 1.2V$, 1.5 Gbps data rate, pre-emphasis off.

FIGURE 2. LLP Performance Characteristics

TRI-STATE and Powerdown Modes

The SCAN15MB200 has output enable control on each of the six onboard LVDS output drivers. This control allows each output individually to be placed in a low power TRI-STATE mode while the device remains active, and is useful to reduce power consumption on unused channels. In TRI-STATE mode, some outputs may remain active while some are in TRI-STATE.

When all six of the output enables (all drivers on both channels) are deasserted (LOW), then the device enters a Powerdown mode that consumes only 0.5mA (typical) of supply current. In this mode, the entire device is essentially powered off, including all receiver inputs, output drivers and internal bandgap reference generators. When returning to active mode from Powerdown mode, there is a delay until valid data is presented at the outputs because of the ramp to power up the internal bandgap reference generators.

Any single output enable that remains active will hold the device in active mode even if the other five outputs are in TRI-STATE.

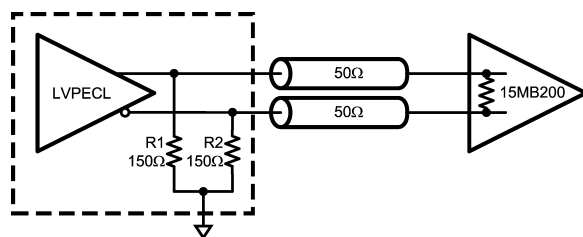
When in Powerdown mode, any output enable that becomes active will wake up the device back into active mode, even if the other five outputs are in TRI-STATE.

Input Failsafe Biasing

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to V_{DD} thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5k Ω to 15k Ω range to minimize loading and waveform distortion to the driver. Please refer to application note AN-1194, "Failsafe Biasing of LVDS Interfaces" for more information.

Interfacing LVPECL to LVDS

An LVPECL driver consists of a differential pair with coupled emitters connected to GND via a current source. This drives a pair of emitter-followers that require a 50 Ω to V_{CC}-2.0 load. A modern LVPECL driver will typically include the termination scheme within the device for the emitter follower. If the driver does not include the load, then an external scheme must be used. The 1.3 V supply is usually not readily available on a PCB, therefore, a load scheme without a unique power supply requirement may be used.

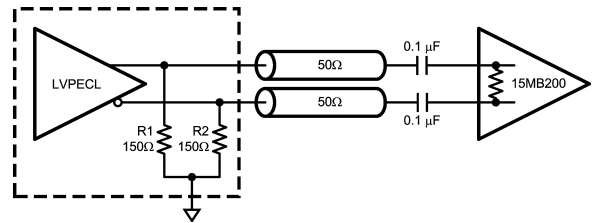


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FIGURE 3. DC Coupled LVPECL to LVDS Interface

Figure 3 is a separated π termination scheme for a 3.3 V LVPECL driver. R1 and R2 provides proper DC load for the driver emitter followers, and may be included as part of the driver device (Note 17). The 15MB200 includes a 100 Ω input termination for the transmission line. The common mode

voltage will be at the normal LVPECL levels – around 2 V. This scheme works well with LVDS receivers that have rail-to-rail common mode voltage, V_{CM}, range. Most National Semiconductor LVDS receivers have wide V_{CM} range. The exceptions are noted in devices' respective datasheets. Those LVDS devices that do have a wide V_{CM} range do not vary in performance significantly when receiving a signal with a common mode other than standard LVDS V_{CM} of 1.2 V.



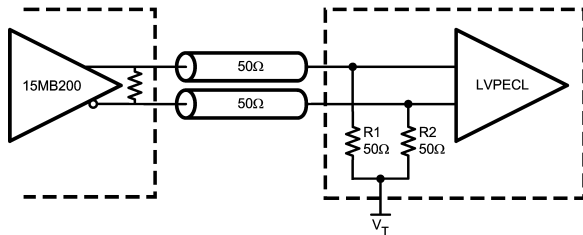
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FIGURE 4. AC Coupled LVPECL to LVDS Interface

An AC coupled interface is preferred when transmitter and receiver ground references differ more than 1 V. This is a likely scenario when transmitter and receiver devices are on separate PCBs. Figure 4 illustrates an AC coupled interface between a LVPECL driver and LVDS receiver. R1 and R2, if not present in the driver device (Note 17), provide DC load for the emitter followers and may range between 140-220 Ω for most LVPECL devices for this particular configuration. The 15MB200 includes an internal 100 Ω resistor to terminate the transmission line for minimal reflections. The signal after ac coupling capacitors will swing around a level set by internal biasing resistors (i.e. fail-safe) which is either V_{DD}/2 or 0 V depending on the actual failsafe implementation. If internal biasing is not implemented, the signal common mode voltage will slowly drift to GND level.

Interfacing LVDS to LVPECL

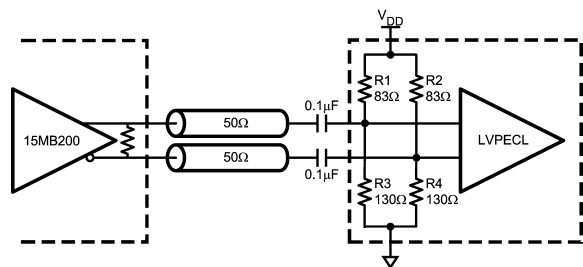
An LVDS driver consists of a current source (nominal 3.5mA) which drives a CMOS differential pair. It needs a differential resistive load in the range of 70 to 130Ω to generate LVDS levels. In a system, the load should be selected to match transmission line characteristic differential impedance so that the line is properly terminated. The termination resistor should be placed as close to the receiver inputs as possible. When interfacing an LVDS driver with a non-LVDS receiver, one only needs to bias the LVDS signal so that it is within the common mode range of the receiver. This may be done by using separate biasing voltage which demands another power supply. Some receivers have required biasing voltage available on-chip (V_T , V_{TT} or V_{BB}).



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FIGURE 5. DC Coupled LVDS to LVPECL Interface

Figure 5 illustrates interface between an LVDS driver and a LVPECL with a V_T pin available. R1 and R2, if not present in the receiver (Note 17), provide proper resistive load for the driver and termination for the transmission line, and V_T sets desired bias for the receiver.



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FIGURE 6. AC Coupled LVDS to LVPECL Interface

Figure 6 illustrates AC coupled interface between an LVDS driver and LVPECL receiver without a V_T pin available. The resistors R1, R2, R3, and R4, if not present in the receiver (Note 17), provide a load for the driver, terminate the transmission line, and bias the signal for the receiver.

Note 17: The bias networks shown above for LVPECL drivers and receivers may or may not be present within the driver device. The LVPECL driver and receiver specification must be reviewed closely to ensure compatibility between the driver and receiver terminations and common mode operating ranges.

Design-For-Test (DfT) Features

IEEE 1149.1 SUPPORT

The SCAN15MB200 supports a fully compliant IEEE 1149.1 interface. The Test Access Port (TAP) provides access to boundary scan cells at each LVTTTL I/O on the device for interconnect testing. Differential pins are included in the same boundary scan chain but instead contain IEEE1149.6 cells. IEEE1149.6 is the improved IEEE standard for testing high-speed differential signals.

Refer to the BSDL file located on National's website for the details of the SCAN15MB200 IEEE 1149.1 implementation.

IEEE 1149.6 SUPPORT

AC-coupled differential interconnections on very high speed (1+ Gbps) data paths are not testable using traditional IEEE 1149.1 techniques. The IEEE 1149.1 structures and methods are intended to test static (DC-coupled), single ended networks. IEEE 1149.6 is specifically designed for testing high-speed differential, including AC coupled networks.

The SCAN15MB200 is intended for high-speed signalling up to 1.5 Gbps and includes IEEE1149.6 on all differential inputs and outputs.

FAULT INSERTION

Fault Insertion is a technique used to assist in the verification and debug of diagnostic software. During system testing faults are "injected" to simulate hardware failure and thus help verify the monitoring software can detect and diagnose these faults. In the SCAN15MB200 an IEEE1149.1 "stuck-at" instruction can create a stuck-at condition, either high or low, on any pin or combination of pins. A more detailed description of the stuck-at feature can be found in NSC Applications note AN-1313.

Packaging Information

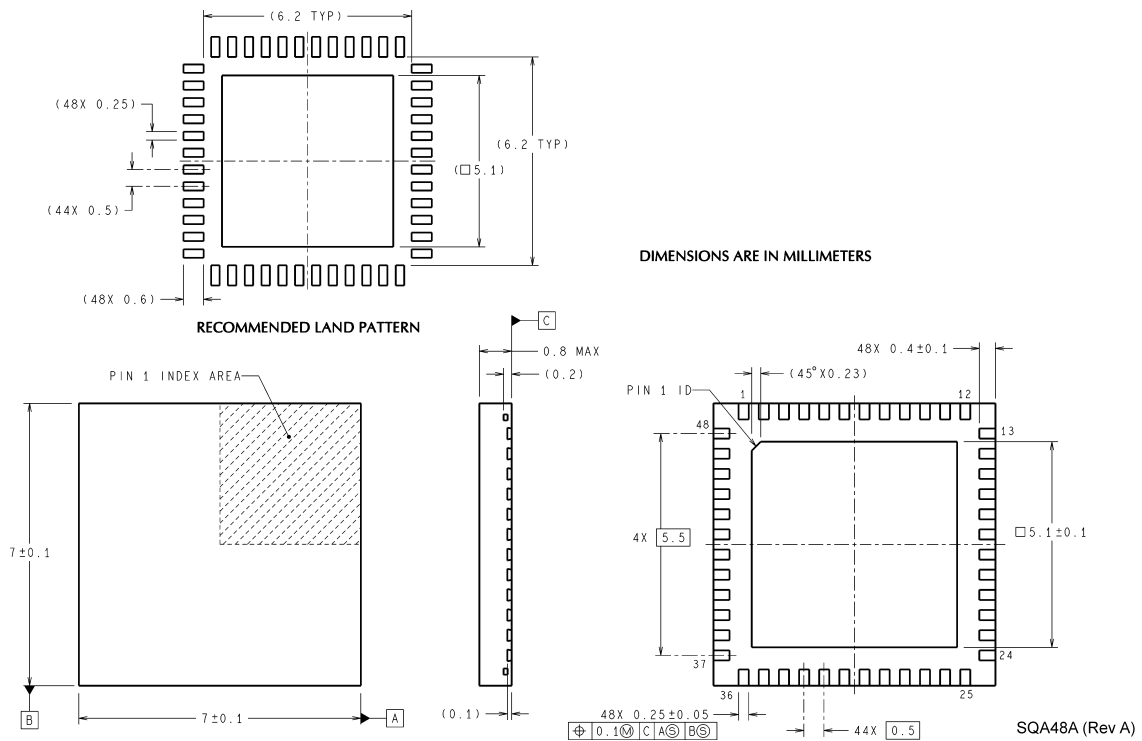
The Leadless Leadframe Package (LLP) is a leadframe based chip scale package (CSP) that may enhance chip speed, reduce thermal impedance, and reduce the printed circuit board area required for mounting. The small size and very low profile make this package ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs. The LLP package is offered in the no Pullback configuration. In the no Pullback configuration the standard solder pads extend and terminate at the edge of the package. This feature offers a visible solder fillet after board mounting.

The LLP has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

For more details about LLP packaging technology, refer to applications note AN-1187, "Leadless Leadframe Package"

Physical Dimensions inches (millimeters) unless otherwise noted



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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor manufactures products and uses packing materials that meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

Leadfree products are RoHS compliant.



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